CLAIMS

1. An integrated circuit comprising:

a first three-terminal device of a first type; and

a second three-terminal device of the first type, a first terminal of the second three-terminal device electrically coupled to a first terminal of the first three-terminal device, and a second terminal of the second three-terminal device electrically coupled to a second terminal of the first three-terminal device,

wherein:

a reference current applied to a third terminal of the second three-terminal device generates a control voltage applied to the second terminals of the first and second three-terminal devices;

where the control voltage is a function of comparing an output voltage at the third terminal of the second three-terminal device to a reference voltage; and

the reference current is derived from the reference voltage and a reference resistance.

2. The integrated circuit of claim 1 wherein:

the second three-terminal device has a different output impedance than the first three-terminal device.

3. The integrated circuit of claim 2 wherein:

the second three-terminal device has a larger output impedance than the first three-terminal device.

4. The integrated circuit of claim 1 further comprising:

a supply voltage electrically coupled to the first terminals of the first and second three-terminal devices.

5. The integrated circuit of claim 1 wherein:

the second terminal of the first three-terminal device is a first control terminal for the first three-terminal device; and

the second terminal of the second three-terminal device is a second control terminal for the second three-terminal device.

6. The integrated circuit of claim 1 further comprising:

a first resistor coupled to a third terminal of the first three-terminal device;

a second resistor coupled to the third terminal of the second three-terminal device; and

an output of the integrated circuit coupled to the first resistor,

wherein:

the reference current is applied to the third terminal of the second three-terminal device through the second resistor; and

the output voltage at the third terminal of the second three-terminal device is measured from the second resistor.

7. The integrated circuit of claim 6 wherein:

an output impedance at the output of the integrated circuit comprises an output impedance of the first three-terminal device and an impedance of the first resistor.

8. The integrated circuit of claim 7 wherein:

the impedance of the first resistor is greater than the output impedance of the first three-terminal device.

9. The integrated circuit of claim 8 wherein:

the output impedance of the integrated circuit is substantially linear across an operating range of an output voltage at the output of the integrated circuit.

10. The integrated circuit of claim 1 further comprising:

an output of the integrated circuit coupled to a third terminal of the first three-terminal device; and

a capacitor coupling the second terminals of the first and second three-terminal devices to the output of the integrated circuit.

11. The integrated circuit of claim 10 wherein:

the capacitor controls a slew rate of an output voltage at the output of the integrated circuit.

12. The integrated circuit of claim 1 further comprising:

a third three-terminal device of the first type, a first terminal of the third three-terminal device electrically coupled to the first terminals of the first and second three-terminal devices, a second terminal of the third three-terminal device removably and electrically coupled to the first and second terminals of the first and second three-terminal devices, and a third terminal of the third three-terminal device electrically coupled to a third terminal of the first three-terminal device; and

a fourth three-terminal device of the first type, a first terminal of the fourth three-terminal device electrically coupled to the first terminals of the first, second, and third three-terminal devices, a second terminal of the fourth three-terminal device removably and electrically coupled to the first terminals of the first, second, and third three-terminal devices and to the second terminals of the first and second three-terminal devices.

13. The integrated circuit of claim 1 further comprising:

an output of the integrated circuit coupled to a third terminal of the first three-terminal device;

a third three-terminal device of the first type, a first terminal of the third three-terminal device coupled to a third terminal of the second three-terminal device, and a third terminal of the third three-terminal device coupled to the second terminals of the first and second three-terminal devices;

an amplifier comprising two inputs and an output, a first one of the two inputs coupled to the third terminal of the second three-terminal device and to the first terminal of the third three-

terminal device, the output coupled to a second terminal of the third three-terminal device, and a second one of the two inputs coupled to the reference voltage; and

a current source providing the reference current and coupled to the third terminal of the third three-terminal device and to the second terminals of the first and second three-terminal devices.

14. The integrated circuit of claim 13 further comprising:

a first resistor coupling the output of the integrated circuit to the third terminal of the first three-terminal device; and

a second resistor coupling the third terminal of the second three-terminal device to the first one of the two inputs of the amplifier and to the first terminal of the third three-terminal device,

wherein:

the reference current is applied to the third terminal of the second three-terminal device through the second resistor and through the third three-terminal device; and

the output voltage at the third terminal of the second three-terminal device is measured from the second resistor.

15. The integrated circuit of claim 13 further comprising:

a capacitor coupling the second terminals of the first and second three-terminal devices, the third terminal of the third three-terminal devices, and the current source to the output of the integrated circuit.

16. The integrated circuit of claim 15 wherein:

the capacitor controls a slew rate of an output voltage at the output of the integrated circuit.

17. The integrated circuit of claim 13 further comprising:

a first resistor coupling the output of the integrated circuit to the third terminal of the first three-terminal device;

a second resistor coupling the third terminal of the second three-terminal device to the first one of the two inputs of the amplifier and to the first terminal of the third three-terminal device; and

a capacitor coupling the second terminals of the first and second three-terminal devices, the third terminal of the third three-terminal devices, and the current source to the output of the integrated circuit and to the first resistor;

wherein:

the reference current is applied to the third terminal of the second three-terminal device through the second resistor and through the third three-terminal device;

the output voltage at the third terminal of the second three-terminal device is measured from the second resistor; and

the capacitor controls a slew rate of an output voltage at the output of the integrated circuit.

18. The integrated circuit of claim 1 further comprising:

an output of the integrated circuit coupled to a third terminal of the first three-terminal device;

an amplifier comprising two inputs and an output, a first one of the two inputs coupled to a third terminal of the second three-terminal device, a second one of the two inputs coupled to the reference voltage, and the output coupled to the second terminals of the first and second three-terminal devices; and

a current source providing the reference current and coupled to the first one of the two inputs of the amplifier and to the third terminal of the second three-terminal device.

19. The integrated circuit of claim 18 further comprising:

a first resistor coupling the output of the integrated circuit to the third terminal of the first three-terminal device; and

a second resistor coupling the third terminal of the second three-terminal device to the first one of the two inputs of the amplifier and to the current source,

wherein:

the reference current is applied to the third terminal of the second three-terminal device through the second resistor; and

the output voltage at the third terminal of the second three-terminal device is measured from the second resistor.

20. The integrated circuit of claim 18 further comprising:

a capacitor coupling the second resistor, the first one of the two inputs of the amplifier, and the current source to the first resistor and to the output of the integrated circuit.

21. The integrated circuit of claim 20 wherein:

the capacitor controls a slew rate of an output voltage at the output of the integrated circuit.

22. The integrated circuit of claim 18 further comprising:

a first resistor coupling the output of the integrated circuit to the third terminal of the first three-terminal device;

a second resistor coupling the third terminal of the second three-terminal device to the first one of the two inputs of the amplifier and to the current source; and

a capacitor coupling the second resistor, the first one of the two inputs of the amplifier, and the current source to the first resistor and to the output of the integrated circuit,

wherein:

the reference current is applied to the third terminal of the second three-terminal device through the second resistor;

the output voltage at the third terminal of the second three-terminal device is measured from the second resistor; and

the capacitor controls a slew rate of an output voltage at the output of the integrated circuit.

23. A driver circuit comprising:

a first MOSFET having a first gate electrode, a first drain electrode, and a first source electrode;

a first resistor coupled to the first drain electrode;

an output of the driver circuit coupled to the first resistor;

a second MOSFET having a second gate electrode, a second drain electrode, and a second source electrode, the first and second gate electrodes coupled together and the first and second source electrodes coupled together;

a second resistor coupled to the second drain electrode;

a third MOSFET having a third gate electrode, a third drain electrode, and a third source electrode, the third source electrode coupled to the second resistor;

an amplifier having a first amplifier input, a second amplifier input, and an amplifier output, the first amplifier input coupled to the second resistor and the third source electrode, the second amplifier input coupled to a reference voltage, and the amplifier output coupled to the third gate electrode; and

a current source coupled to the third drain electrode, the first gate electrode, and the second gate electrode.

24. The driver circuit of claim 23 wherein:

the second MOSFET has a larger output impedance than the first MOSFET; and

the second resistor has a larger impedance than the first resistor.

25. The driver circuit of claim 24 wherein:

an output impedance of the driver circuit at the output of the driver circuit comprises an output impedance of the first MOSFET and an impedance of the first resistor;

the impedance of the first resistor is greater than the output impedance of the first MOSFET such that the output impedance of the driver circuit is substantially linear.

26. The driver circuit of claim 25 further comprising:

a capacitor coupling output of the driver circuit to the third drain electrode, the first and second gate electrodes, and the current source to control a slew rate of an output voltage at the output of the driver circuit.

27. The driver circuit of claim 25 further comprising:

a fourth MOSFET having a fourth gate electrode, a fourth drain electrode, and a fourth source electrode, the fourth drain electrode coupled to the first resistor and the first drain electrode, and the fourth source electrode coupled to the first and second source electrodes; and

a first switch coupling the fourth gate electrode to the first and second gate electrodes and the current source.

28. The driver circuit of claim 27 further comprising:

a fifth MOSFET having a fifth gate electrode, a fifth drain electrode, and a fifth source electrode, the fifth drain electrode coupled to the first resistor and the first and fourth drain electrodes, and the fifth source electrode coupled to the first, second, and fourth source electrodes;

a second switch coupling the fifth gate electrode to the first and second gate electrodes and the current source;

a third switch coupling the fifth gate electrode to the first, second, fourth and fifth source electrodes; and

a fourth switch coupling the fourth gate electrode to the first, second, fourth, and fifth source electrodes.

29. The driver circuit of claim 28 further comprising:

a capacitor coupling the output of the driver circuit and the first resistor to the first and second gate electrodes, the third drain electrode, and the current source to control a slew rate of an output voltage at the output of the driver circuit.

30. The driver circuit of claim 29 further comprising:

a fifth switch coupling the first and second gate electrodes, the capacitor, the third drain electrode, and the current source to the first, second, fourth, and fifth source electrodes,

wherein:

the first and third switches are simultaneously opened and closed; and

the second and fourth switches are simultaneously opened and closed.

31. An integrated circuit comprising:

a voltage-mode driver circuit having an integral, analog on-chip termination.

32. The integrated circuit of claim 31 wherein:

the voltage-mode driver circuit has a substantially constant output impedance within an operating range of an output voltage of the voltage-mode driver circuit.

33. A method of controlling output impedance of a driver circuit comprising:

generating a reference voltage as a function of a reference current and a reference resistance;

using a first sub-circuit to generate the output impedance of the driver circuit;

using a second sub-circuit with a feedback loop to generate a control voltage; and

using the control voltage to control the output impedance.

34. The method of claim 33 wherein:

the second sub-circuit is a replica of the first sub-circuit.

35. The method of claim 34 wherein:

the second sub-circuit is a scaled replica of the first sub-circuit.

36. The method of claim 33 wherein:

using the control voltage further comprises adjusting the control voltage to keep the output impedance substantially linear across an operating range of an output voltage of the driver circuit.

37. A method of controlling output impedance of a driver circuit comprising:

generating a reference current as a function of a reference voltage and a reference resistance;

using a first sub-circuit to generate the output impedance of the driver circuit;

using a second sub-circuit with a feedback loop to generate a control current; and

using the control current to control the output impedance.

38. The method of claim 37 wherein:

the second sub-circuit is a replica of the first sub-circuit.

39. The method of claim 38 wherein:

the second sub-circuit is a scaled replica of the first sub-circuit.

40. The method of claim 37 wherein:

using the control voltage further comprises adjusting the control voltage to keep the output impedance substantially linear across an operating range of an output voltage of the driver circuit.